Applicants : San Wong and K Application No. : Not yet assigned : San Wong and Kaiyu Ren Docket No. : 174/297 Filed Concurrently herewith

Title BIT ERROR RATE TESTER IMPLEMENTED IN A PROGRAMMABLE LOGIC DEVICE

. 4

Sheet 1 of 4 Agent : Alexander Shvarts, Reg. No. 47,943

100 120 122 102 **Transceiver** 104 132 116 106 **Formatter Formatter** 114、 108 Comparer **Transmitter** Memory **Memory** 110 118 Comparison **Test** Data Data 112 Controller 130

FIG. 1

User

**Equipment** 

126

124

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PROGRAMMABLE LOGIC DEVICE

Agent : Alexander Shvarts, Reg. No. 47,943 Sheet 2 of 4

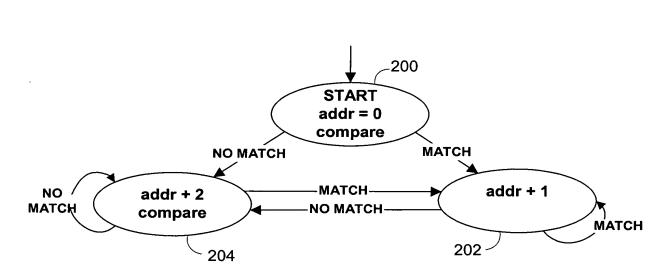


FIG. 2

olicants : San Wong and Kaiyu Ren Docket No. : 174/297

Applicants : San Wong and Kaiyu F
Application No. : Not yet assigned
Filed : Concurrently herewith

Title : BIT ERROR RATE TESTER IMPLEMENTED IN A

PROGRAMMABLE LOGIC DEVICE

Agent : Alexander Shvarts, Reg. No. 47,943 Sheet 3 of 4

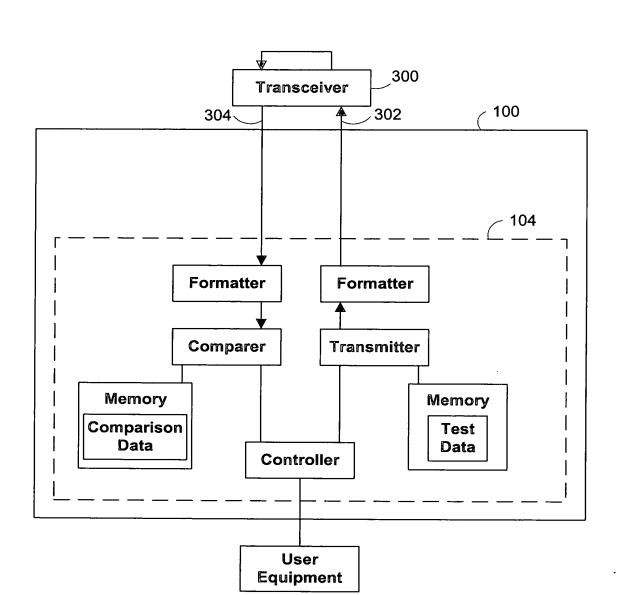


FIG. 3

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: BIT ERROR RATE TESTER IMPLEMENTED IN A Title

PROGRAMMABLE LOGIC DEVICE

Sheet 4 of 4 Agent : Alexander Shvarts, Reg. No. 47,943

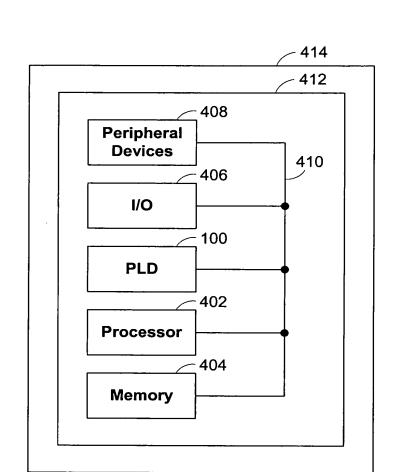


FIG. 4